ABSTRACT

A circuit and a method for self refresh of DRAM cells are provided. The circuit comprises a bias generator and an oscillator. The bias generator comprises a first current generator, a second current generator and a converter. The first current generator generates a first leakage current of "0" state cells. The second current generator generates a second leakage current of "1" state cells. The converter transforms a current comprising the first leakage current and the second leakage current into output biases. The method comprises generating leakage currents from memory cells; transforming the leakage currents into output biases for determining a self refresh period; and using the output biases to control an oscillator for generating a periodical signal pulse in response to the leakage currents.